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10/667,899	09/23/2003	Akiharu Miyanaga	07977-254003 / US3823D1D1	8644
26171 7590 04/09/2009 FISH & RICHARDSON P.C. P.O. BOX 1022 MINNEAPOLIS, MN 55440-1022			EXAMINER VU, DAVID	
			ART UNIT 2818	PAPER NUMBER
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATDOCTC@fr.com



## DETAILED ACTION

### Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 39 and 59 are rejected under 35 U. S. C. 102(b) as being anticipated by Shimizu et al. (US Pat. 5,217,910, hereinafter Shimizu).

**Regarding claims 39 and 59**, Shimizu discloses in figs. 9E a semiconductor device comprising:

a. semiconductor substrate 21;

a channel region formed in semiconductor substrate 21; wherein channel region is located between source and drain regions p;

at least first and second impurity regions 37 formed in channel region wherein first impurity region 37 (left side of the gate) is in contact with the p-source, second impurity region 37 (right side of the gate) is in contact the p-drain region, and first and second impurity regions are doped (n-type) with an impurity of a conductivity type opposite to source region and drain region (p-type)

at least third and fourth impurity regions 31 (n<sup>-</sup>-doped regions) formed in semiconductor substrate wherein third and fourth impurity regions 31 are **electrically** in contact with the source/drain regions (p-doped regions) and are separated from each other and wherein a

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conductivity type of third and fourth impurity regions (n-type) are opposite to that of source and drain regions (p-type)

a gate insulating film formed over the channel region; and

a gate electrode 28 over the channel region with the gate insulating, film interposed therebetween, wherein first (left side) and second (right side) impurity regions are separated from each other.

### **Claim Rejections - 35 USC § 103**

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

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2. Claims 40-42 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Shimizu (US Pat. 5,217,910).

Shimizu discloses a but fails to disclose the concentration of the first, second impurity region is about  $1 \times 10^{17}$  to  $5 \times 10^{19}$  atoms/cm<sup>3</sup> (claim 40); the width of first, second impurity regions along boundary is 0.05 to 0.3  $\mu\text{m}$  (claim 41); the interval between first and second impurity regions is 0.04 to 0.6  $\mu\text{m}$  (claim 42). It appears that having a specific width/ interval and concentration of the impurity regions as claimed is prima facie obvious due to the fact that one can vary the width/ interval and concentration of the impurity regions in order to achieve a specific MOSFET device. Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combined process of Shimizu in view of Sanchez by selecting a suitable the width/ interval and concentration, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955). Moreover, as the width/ interval and concentration of the impurity regions does seem to be critical to the invention, it must be shown that any one or all of the listed materials yield an unexpected product or result. *In re Margolis* 228 USPQ 940 (Fed. Cir. 1986); *In re Kirsch* 182 USPQ 286 (CCPA 1974); *In re Suether* 181 USPQ 36 (CCPA 1974); *In re Costello* 178 USPQ 290 (CCPA 1973); *In re Von Schickh* 150 USPQ 300 (CCPA 1966); *In re Sussman* 60 USPQ 538 (CCPA 1944); *In re Kaplan* 45 USPQ 175 (CCPA 1940).

### **Allowable Subject Matter**

3. Claims 43-58 and 60-61 are allowed.

The following is an examiner's statement of reason for allowance: the prior art of record, either singularly or in combination, does not disclose or suggest a semiconductor device comprising: at least first and second impurity regions formed in said channel region, wherein said first and second impurity regions are in contact with the source region (or wherein said first and second impurity regions are in contact with the drain region) and are separated from each other; wherein each of said first and second impurity regions is doped with an impurity of a conductivity type opposite to that of said source and drain regions.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

### **Response to Arguments**

4. Applicant's arguments with respect to the pending claims have been considered but are moot in view of the new ground(s) of rejection. Although the same reference is applied (Shimizu & Sanchez), the rejections are based on a new interpretation of that reference. Therefore, the arguments presented in response to the interpretation used in the previous Office Action are no longer applicable.

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**Claim 39 requires:**

- a) first impurity region is in contact with the source, second impurity region is in contact the drain region, and first and second impurity regions are doped with an impurity of a conductivity type opposite to source region and drain region, **OR**
- b) both first and second impurity region are in contact with the source, and first and second impurity regions are doped with an impurity of a conductivity type opposite to source region and drain region, **OR**
- c) both first and second impurity region are in contact with the drain, and first and second impurity regions are doped with an impurity of a conductivity type opposite to source region and drain region.

**Conclusion**

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be

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calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Vu whose telephone number is (571) 272-1798. The examiner can normally be reached on Monday-Friday from 8:00am to 5:00pm. If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke H can be reached on (571) 272-1657. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR, Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/DAVID VU/  
Primary Examiner, Art Unit 2818